ratus 26 may further include an IR filter 41 interposed along the optical axis of camera 10 between lens 15 and CCD 19. Filter 41 blocks IR radiation so the charge pattern produced by CCD 19 is more closely related to impinging radiation in the visible spectrum. Factors affecting CCD performance are discussed in *IEEE Transactions On Electron Devices*, Vol. ED-18, No. 11, November 1971, page 986, entitled "Charge-Coupled Imaging Devices: Design Considerations", by G. F. Amelio et al.

As soon as electrical power is applied to circuit 24, CCD 19 immediately begins to produce its pulsed electrical output signals. For successive 50ms exposure intervals families of pulse trains are generated with each pulse train representing the optical image formed during one such interval. Until momentary, pushbutton switch S_2, mounted on camera 10, is depressed, however, circuit 27 is effectively disabled, and image data is not transmitted to apparatus 30 for recording. Circuit 27, in effect, operates as an electronic shutter or gate. However, unlike a conventional camera shutter which operates to control the time during which light is allowed to reach a light-sensitive medium, i.e. film, this electronic shutter controls the signal, representing an optical image, that is to be recorded. The reason circuit 27 is effectively disabled immediately after power is applied to circuitry 24 is to permit CCD 19 to clear itself of thermal charge prior to recording an image signal. With out presently preferred CCD apparatus, we have found that approximately one-half second is needed to clear the CCD of such charge after power is applied.

Circuit 27 operates as follows: Momentary closure of switch S_2 causes a bistable circuit 42 to produce a logic "1" signal at its output 43. A flip flop 44 produces both logic "1" and "0" signals at its output following the occurrence of odd numbered and even numbered pulses, respectively, in the aforementioned 20Hz signal 22. Accordingly, an AND gate 45, which conducts in response to logic "1" signals at each of its inputs, produces a logic "1" output signal following the occurrence of the first odd numbered pulse in signal 22, after switch S_2 is actuated. The logic "1" signal turns ON a conventional sample-and-hold circuit 46. Circuit 46 serves to extend the duration of each pulse in waveform B for the period between the trailing edge of one pulse and the leading edge of the next pulse. Accordingly, sample-and-hold circuit 46 produces an electrical signal having a series of contiguous pulses. Such a signal is denoted by the letter C in FIG. 2. When the output signal produced by gate 45 returns to a logic "0" state, such as when the next pulse (an even numbered pulse) in signal 22 is applied to flip flop 44, circuit 46 is turned OFF. At that time, however, 50ms have passed and an electrical signal representative of a full scene image has been transmitted through sample-and-hold circuit 46.

When the output of gate 45 is a logic "0", a logic "1" signal occurs at the output of a bistable circuit 47. This logic "1" operates to reset circuit 42 so that its output returns to its normal, logic "0" state. This is done to prevent the output of gate 45 re-enabling circuit 46 upon the occurrence of the next odd numbered pulse in waveform 22, without the reactuation of switch S_2.

The aforementioned high frequency signal 23 from CCD address circuit 38 is used to synchronize the operation of sample-and-hold circuit 46 with waveform B. A delay circuit 48 delays signal 23 to allow for CCD readout and signal delay through amplifier 40. Signal 23 is delayed by circuit 48 to synchronize the operation of sample-and-hold circuit 46 with the occurrence of each pulse in waveform B so that pulses are extended at the proper point in time and with the correct amplitude.

Waveform C is applied to A/D converter 28 which converts each extended pulse into a 4-bit digital word having a magnitude representative of pulse amplitude. Converter 49 produces these bits sequentially, the most significant bit is produced first on output 49*a*, and the least significant bit is produced last on output 49*d*. A start-conversion signal is supplied on conductor 50 to permit converter 49 to commence each signal conversion operation in synchronism with the occurrence of each waveform C pulse. This is done by means of signal 23 which is delayed a predetermined amount by a delay circuit 51.

A digital latch 54 is provided to ensure that the bits representing each digital word are not changing during signal transmittal to buffer circuitry 29. A/D converter 28 produces an end-of-conversion (EOC) signal on conductor 56 once each least significant bit is produced, to signal latch 54 to transmit a digital word to buffer 29.

Buffer circuitry 29 constitutes means for receiving signals in the form of digital words from A/D converter 28 in real time, and transmitting such words at a rate that is substantially lower than the rate at which these words are received from the A/D converter. Since digital words representing a single optical image are loaded into memory 58 within 50ms, while approximately 23 seconds are used to transmit such words from the memory to recording apparatus 30, buffer 29 operates to reduce by a factor of approximately 460 the rate that digital words are transmitted to apparatus 30 from the buffer compared to the rate such words are transmitted from the CCD into the buffer. To accomplish this, the buffer 29 includes a highspeed digital memory 58 for temporarily storing words as they are accumulated prior to transmittal from the buffer to recording apparatus 30. Preferably, buffer 29 is operated to transmit stored words after memory 58 has received the last word. This is done to simplify the operation of buffer 29 and does not operate to significantly increase the time between when the signal is produced by CCD 19 and when such signal is recorded by apparatus 30 since all words are loaded into memory 58 within 75ms after an exposure interval commences. It shall be understood, however, that it is within the spirit and scope of our invention that signal transferral from memory 58 can commence as soon as the first digital word is loaded into memory.

Buffer 29 operates as follows: The aforementioned EOC signal produced on conductor 56 is also applied to a memory address counter 60 included within buffer 29. Counter 60 serves a record keeping function for memory 58 by providing an addressenable signal along input address line 61 to control where in memory either write or read operations are to occur. Address counter 60 is initialized to ZERO when AND gate 45 switches its output either from a logic "0" to a logic "1" or from a logic "1" to a logic "0". When an EOC signal is produced, counter 60 increments its count by one to permit the memory location corresponding to that count or address to receive a digital word for storage.

A memory control circiut 62 provides command signals to memory 58 to control whether information is to be written into a read from memory. Control circuit 62 is enabled to produce memory write-control and read-control signals on conductor 63a when the output

of gate 45 is a logic "1" and a logic "0", respectively. These write-control and read-control signals turn input write-logic and read-logic gates (not shown) ON in memory 58 to permit data to be written or read, respectively, from memory at the address corresponding to the count provided by counter 60. Such write-control and read-control signals are produced when data-ready signals are provided on input conductor 63c. These data-ready signals occur either when the aforementioned EOC signals are produced, or when recording apparatus 30 produces its output signals, as explained in detail hereinafter.

Memory 58 is comprised of a plurality of solid-state random access memories (RAM's) which are connected together to provide high-speed storage for 10,000 4-bit words within the aforementioned 50ms interval. Solid-state memories have the speed for storing data this quickly. However, as is known in the art, solid-state RAM's may periodically require "rejuvenation" or "refreshing" to maintain data as originally stored. Buffer 29 therefore, includes memory refresh circuitry comprising a refresh-request circuit 66, under the control of an oscillator 68, and a refresh address counter 70. Circuit 66 produces a refresh-request signal on conductor 66a, and counter 70 produces a refresh-address signal on conductor 70a. Each of such signals are produced at 63 microsecond intervals. The refresh-address signal determines which memory locations are to be refreshed. Each refresh-request signal causes memory control 62 to produce a memory refresh signal on conductor 63b to refresh the data at the memory address corresponding to the count provided by counter 70.

The circuitry within memory 58 by which stored information is refreshed, and information is stored and/or written into the memory is readily available commercially. In our preferred embodiment, memory 58 is comprised of dynamic RAM's manufactured by the Motorola Corporation, and designated MCM6605.

An information storage device that requires electrical power to retain or preserve stored information presents obvious advantages, particularly for camera users who wish to store recorded information for long intervals. Accordingly, it is desirable to provide a storage device by which scene information may be permanently stored or recorded without the need for electrical power to preserve the information once it is recorded. A storage device of this type is known in the art as non-volatile. In addition, it is desired that such a storage device be inexpensive. To meet these objectives, buffer memory 29 includes circuitry for outputting stored data at a rate below the 200 KHz rate, e.g. 10,000 words within the 50ms interval, that data is received. The desired data output rate is controlled so that it is compatible with the recording speed of a permanent inexpensive recording apparatus, such as, for example, an audiograde magnetic tape recorder. Such circuitry controls the rate data is read from memory 58 and includes a clock 71, a parallel-to-serial bit converter 72, and sync-pulse generator 73. Generator 73 is controlled by clock 71 and produces at its output 75 both a sync signal to be recorded and a data-ready signal to read stored information from the memory.

Recording apparatus 30 includes, in addition to cassette 20, a tape recorder motor 76, a motor speed monitor circuit 77, a voltage-sensitive trigger circuit 78, and a bistable circuit 79. When switch S_2 is closed, bistable circuit 79 produces a logic "1" signal at its output to turn motor 76 ON to drive the tape in cassette 20. Data commences to be read from memory 58 to be recorded on the tape once both tape recorder motor 76 is operating above a predetermined speed, and the last digital word has been stored in buffer 29. Since motor 76 does not reach such speed instantaneously following the actuation of switch S_2, motor speed monitoring circuit 77 is provided to produce a voltage signal having an amplitude proportional to motor speed. This voltage signal is applied to the input of voltage-sensitive trigger circuit 78. Circuit 78 is of the type known in the art as a Schmitt trigger circuit that produces a low-level voltage at its output when a voltage is present at its input that is less than a predetermined level. Likewise, when a voltage signal applied to its input exceeds a predetermined threshold, a high-level voltage signal is produced at its output that is applied to one of two inputs to an AND gate 80.

In addition, when AND gate 45 switches its output from a logic "1" to a logic "0", indicative of when a full scene image has been transmitted through circuit 46 and, accordingly, into buffer 29, a high-level signal is applied to the second of the two inputs to AND gate 80. It would be necessary to invert the logic "0" signal at the output of gate 45 if such signal were a low-level signal. This could, of course, be done by means of an inverter circuit (not shown).

AND gate 80 conducts in response to high-level signals at each of its inputs. Accordingly, gate 80 produces an output signal once motor 76 is operating above a predetermned speed, and a full scene image has been loaded into buffer 29.

When AND gate 45 switches its output from a logic "1" to a logic "0", control circuit 62 is enabled to produce the aforementioned read-control signal when a data-ready signal occurs on conductor 63c. In a manner similar to when a write-control signal is produced, circuit 62 produces voltage signals to set input read-logic gates (not shown) to permit data to be read from memory 58.

Recording apparatus 30 begins to record data stored in buffer 29 once AND gate 80 produces its ouput signal. Such signal causes a one-shot multivibrator 81 to produce an output pulse that is applied to OR gate 82. When this occurs, memory address counter 60 is caused to increment its count by 1. In addition, a data-ready signal is applied to control circuit 62 along conductor 63c. This signal causes control circuit 62 to produce a read-control signal which is applied to memory 58 along conductor 63c. When this happens, a 4-bit word is read out of memory 58 in parallel bit form, at the address determined by counter 60, and is applied to parallel-to-serial bit converter 72. Each 4-bit word is converted to a 4-bit word in serial form and transmitted to tape cassette 20 for recording. At the same time, sync-pulse generator 73 produces a sync bit which is added to the 4 serial bits to produce a 5-bit word that is recorded on magnetic tape loaded in cassette 20.

Each sync pulse is also applied to OR gate 82 to initiate a subsequent read-control signal and to increment address counter 60 by one. The preceding data read sequence continues until each of the 10,000 4-bit words are read from memory and recorded on magnetic tape. Once the last word is recorded, OR gate 82 increments counter 60 to 10,001. When this occurs, and AND gate 84 produces a high-level voltage signal that is applied to input 36 of flip flop 34. Accordingly, flip flop 34 produces a low-level voltage at its output 35 and transistor 37 turns OFF, thereby removing electrical

power from camera 10. by automatically turning camera 10 OFF, inadvertent power drain from camera battery 31 is prevented.

Additional pictures are recorded by sequentially reactuating buttons S_1, S_2. However, cassette 20 may be removed from camera 10 after any number of scenes have been recorded.

In a presently preferred embodiment tape recorder apparatus 30 records scene information at a data rate of approximately 2,150 bits/second. Since 5 bits are used to represent the scene light sensed at each of 10,000 photosites (4 information bits and 1 sync bit) 50,000 total bits are used to record each picture. Consequently, an electrical signal representative of a single scene is read from memory 58 and is magnetically recorded in approximately the aforementioned 23 seconds. The recording rate of 2,150 bits/second resulted from a recording density of 390 bits/inch on the tape and a maximum tape speed of 5.5 inches/second. There are, of course, other audio-grade recording systems that would utilize tape having an inherently higher recording density and/or a higher tape speed and which would accordingly reduce the time for magnetically recording a scene. In addition, source and/or channel encoding schemes could be employed to more efficiently record information on the tape. With our presently preferred audiograde tape recorder, up to 25 pictures can be recorded on a single cassette tape.

There is shown in FIG. 4 an arrangement by which recorded scene information may be displayed for viewing. Such an arrangement includes a microcomputer 86 of the type manufactured by the Motorola Corporation, and a conventional TV monitor 88. Microcomputer 86 reads scene data from cassette 20 and temporarily stores it in an internal memory (not shown). Microcomputer 86 also reorganizes the data so that it is not presented for display with the same interlaced timing format that data is read out of CCD 19. Digital words are converted to analog form and arranged in a TV-scan format for display on monitor 88. Apparatus, such as microcomputer 86, for converting information data to a format suitable for TV display are well known in the art.

One advantage of the arrangement shown in FIG. 4 is that the camera operator may first visually display each recorded scene, then decide whether to keep the picture. Unwanted scenes may be erased from the tape, and the tape may be reused without incurring additional cost.

Permanent photographic prints may be made on conventional photographic paper. This can be done using electrooptical signal translating apparatus. For example, scene information may be read from magnetic tape and reconverted into a pulsed electrical signal, such as the aforementioned waveform C. Individual pulses in waveform C would then be applied to timing circuitry for controlling the time duration that photographic paper would be exposed. Since each pulse is related to the brightness of a particular point in the recorded scene, the photographic paper may be exposed by a series of variable-duration light signals from a light beam scanned across the paper.

While we have described our invention as employing a magnetic tape for low cost non-volatile information storage, it shall be understood that other non-volatile informationstorage media may be utilized. We prefer to use a non-volatile storage device for user convenience and to reduce power consumption. One other storage medium that appears very attractive for meeting these criteria is a magnetic bubble device. This type of storage device is attractive not only because it is basically non-volatile and requires low power, but offers the further advantage of large storage capacity and may potentially be used to store millions of bits in one device. If this were the case, a magnetic bubble device could replace the magnetic tape recorder.

Although various specific elements and data handling capabilities and characteristics have been used to describe our electronic camera invention, it shall be understood by those skilled in the art that numerous modifications may be made that are within the spirit and scope of our inventive contribution. For example, picture quality could be improved with the use of more bits per photosite to produce improved scene contrast. In an article by A. A. Goldberg, entitled "PCM Encoded MTSC Color Television Subjective Tests", and appearing in *SMPTE*, Vol. 82, No. 8, August 1973, it was reported that no noticeable degradation of picture quality (on an NTSC 525-line, 60-field TV signal) occurred when 6 bits per photosite were used, compared to a picture produced with an undigitized signal.

Furthermore, color pictures are possible using multiple CCD's with appropriate filters or with the development of a single, color responsive CCD. For "capturing" color images, an electrical signal for each of three primary colors could be produced in a manner as set forth hereinbefore. Recorded scene information may be displayed for viewing by transforming each signal into its corresponding color, and forming a composite polychromatic picture. For a detailed description of a solidstate color imaging device, reference is made to U.S. Pat. No. 3,971,065, entitled COLOR IMAGING ARRAY, and assigned to the assignee of the present invention.

Electronic imaging apparatus within the teachings of our invention provides a user the opportunity to take pictures in available light. By utilizing other CCD properties, other advantages can be realized. For example, IR photography is possible with the same camera by simply filtering the light before it reaches the CCD.

In addition, although we have described a preferred embodiment of our invention as constituting an electronic still camera, it shall be understood that the essence of our inventive contribution is also applicable to other electronic imaging apparatus such as, for example, apparatus for recording fast-action scenes such as movie camera apparatus.

We claim:

1. In an electronic still camera having a solidstate light-responsive device for producing at a relatively high rate a stream of discrete signals indicative of optical images received by said device during adjacent exposure intervals, the improvement comprising:

(a) means for extracting said discrete signals from said light-responsive device during a time interval which is no greater than the interval during which said optical images are produced;

(b) circuit means for separating said signals from each other;

(c) means for transforming said separated signals into a stream of signals occurring at a rate which is slower than said high rate; and

(d) means for recording in real time on a non-volatile medium said slower rate stream of signals.

2. Apparatus as set forth in claim 1 wherein said transforming means comprises storage means for enabling production of said high rate stream of signals and re-

cording of said slower rate stream of signals to occur concurrently.

3. In an electronic still camera having a solid-state light-responsive device located to receive an optical image, said light-responsive device including electrical addressing means for producing families of electrical signals relating to charge patterns formed in said light-responsive device during successive exposure intervals, each signal within a family corresponding to a charge pattern formed during one exposure interval and each of said signals defining a first train of information bearing indices occurring at a first relatively high rate, the improvement comprising:

(a) control means for providing a signal to said electrical addressing means to extract said families of electrical signals from said lightresponsive device at a speed which is at least as great as the speed at which said charge patterns are formed;

(b) electrical gating means for effectively isolating at one of said electrical signals from the other of said electrical signals;

(c) means associated with said gating means for transforming the electrical signal which has been isolated into a second train of information bearing indices occurring at a rate which is substantially less than said first rate of said first train of information bearing indices; and

(d) means for recording on a medium said second train of information bearing indices.

4. In an electronic still camera having a solid-state imaging device located at an exposure plane, means associated with said imaging device for forming charge patterns relating to optical images projected onto said imaging device during adjacent exposure intervals, the improvement comprising:

(a) means for producing a stream of discrete electrical signals, representative of said charge patterns, at a speed which is at least as great as the speed at which said charge patterns are formed;

(b) electrically energizable circuit means for separating a one of said electrical signals from the other of said electrical signals;

(c) means responsive to said separated electrical signal for producing a plurality of multi-bit words indicative of said separated electrical signal, said digital words being produced in real time;

(d) data storage means;

(e) means for transferring said digital words into said data storage means in real time at a first relatively high rate;

(f) means for retrieving said digital words from said data storage means at a second rate that is substantially lower than said first relatively high rate; and

(g) recording apparatus for recording said retrieved digital words on a non-volatile recording medium, said recording apparatus having a recording speed that is compatible with said second rate.

5. In an electronic still camera having a light-responsive device located at an exposure plane for producing charge patterns relating to optical images projected onto said light-responsive device during adjacent exposure intervals, the improvement comprising:

(a) control means for providing a signal;

(b) electrical addressing means associated with said light-responsive device and responsive to said signal for extracting from said light-responsive device information-bearing electrical signals corresponding to said charge patterns at a speed which is at least as great as the speed at which said charge patterns are formed;

(c) electronic shutter control means having (1) a first state for blocking transmittal of said electrical signals, and (2) a second state for transmitting a one of said electrical signals;

(d) actuatable means for switching said control means from its state into its second state;

(e) a signal storage device for receiving and storing in real time at a first data rate representations corresponding to said transmitted electrical signal;

(f) means for retrieving said representations from said signal storage device at a second data rate that is substantially less than said first rate; and

(g) recording apparatus for recording said representations on a non-volatile recording medium, said recording apparatus having a recording speed that is suitable for recording said representations at the rate at which said representations are retrieved from said signal storage device.

6. An electronic still camera as set forth in claim 5 including means for automatically switching said control means from said second state back to said first state following transmittal of said information-bearing electrical signal.

7. In an electronic still camera having a solid-state light-responsive imaging device located to receive optical images, the improvement comprising:

(a) electrical addressing means associated with said imaging device for producing families of electrical signals derived from optical images formed on said imaging device during adjacent exposure intervals, each signal within a family corresponding to an optical image formed during one exposure interval and said signals being produced at a first rate which is at least as great as the rate at which said optical images are formed;

(b) electrical gating means having (1) a first state for blocking transmittal of said electrical signals, and (2) a second state for transmitting said electrical signals;

(c) switching means synchronized with said electrical addressing means for switching said electrical gating means from said first state into said second state then back to said first state for transmitting a given one of said electrical signals;

(d) means for temporarily storing representations of said transmitted electrical signal in real time and for retransmitting said representations at a second rate that is substantially less than said first rate; and

(e) recording apparatus for recording said representations on a non-volatile recording medium, said recording apparatus having a signal access speed that is compatible with the second rate at which said representations are retransmitted.

8. In an electronic still camera including a charge coupled device defining an array of light-sensitive elements located at an exposure plane, the improvement comprising:

(a) electrical addressing means associated with said light-sensitive elements for producing families of pulsed electrical signals relating to optical images projected onto said elements during contiguous exposure intervals, said signals being produced at a rate which is at least as great as the rate at which said optical images are formed;

(b) an electrical gating means having (1) a first state for blocking transmittal of said pulsed electrical

signals, and (2) a second state for transmitting said electrical signals;

(c) actuatable switching means for switching said gating means from said first state into said second state;

(d) said electrical gating means including means for automatically switching said gating means from said second state back to said first state following transmittal of the first one of said electrical signals which occurs after actuation of said switching means;

(e) a digital data storage device;

(f) converter means for converting in real time said pulses in said first one of said electrical signals into a multi-bit digital word;

(g) means for transferring said digital words in real time into said digital data storage device;

(h) means for retrieving said digital words from said data storage device at a rate that is more than an order of magnitude less than the rate at which said words are transferred into said storage device; and

(i) recording apparatus coupled to said digital words retrieving means for recording said digital words on a magnetic recording medium, said recording apparatus having a recording speed that is compatible with recording signals at an audio-grade recording rate.

* * * * *

C-012 through C-048

Have Been Redacted for Confidentially

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

AMPEX CORPORATION,	)	
Plaintiff,	)	
v.	)	C.A. No.
EASTMAN KODAK COMPANY, et al.,	)	04-1373 (KAJ)
Defendants.	)	

Videotaped Deposition of

GEORGE T. LIGLER, Ph.D.

Washington, D.C.

Wednesday, May 10, 2006

9:35 a.m.

Job No.: 22-77797

Pages 1 - 341, Volume 1

Reported By: Joan V. Cain

part of the schematics. We can check.

Q Did the Ampex product have a CCD?

MR. BEAMER: Objection, vague.

A I don't know.

BY MR. LEE:

Q Have you ever heard of the phrase "CFA interpolation"?

A Yes, sir.

Q Do you understand what CFA interpolation is?

A Generally, yes, sir.

Q What is CFA interpolation?

A CFA interpolation is where the values of pixels in a CFA array are -- are used to derive for each pixel that is being represented, R, G, and B -- I'm talking R -- RGB interpolation here, R, G, and B color components for that pixel.

Q Now, is it true that CFA interpolation is implemented by an algorithm?

A Yes.

Q A mathematical algorithm, correct?

A Yes.

Q Have you ever been retained to consult -- strike that.

before I thought the initial digital cameras came out. So I want to be precise in my answer.

Q Who invented the digital camera?

A I don't know.

Q You have no idea?

A Well, I know that an initial digital camera came out sometime in the early '80s, 1981, perhaps a year or two earlier than that.

Q Do -- do you have any idea who the industry credits with having brought the first digital -- developed the first digital camera?

A I think I have an -- well, the first commercially available one -- I think it's somewhere in one of my reports but --

Q Well my question --

A Go ahead.

Q This case is all about digital cameras, right?

A Right.

Q My question to you is, do you have any idea who invented the digital camera?

A I don't know who invented the digital camera.

Q Have you ever heard of a man named Steve

digital cameras.

Q Was the phrase "digital camera" known before April 8th, 1983?

A Yes.

Q Were there patents before April 8th, 1983 that used the phrase "digital camera"?

A I haven't checked. I don't know. I -- I would assume there were, sir, but I don't know.

Q Do you have patents issued in your name?

A No.

Q Okay. You do have publications though, correct?

A Sure do.

Q Do any of them use the word "digital camera"?

A That's a good question. One of them may, but I don't think so.

Q Do any of them address any design aspects of digital cameras?

A No, sir.

Q Do any of them describe the implementation of algorithms in digital cameras?

A No, sir, they don't.

Q When is the first time that you read a